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Commissioner for Patents, Washington, D.C. 20231.

Parson 3-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): D.E. Parson et al.

Case:

3-2-1-4

Serial No.: Filing Date: 09/583,057 May 30, 2000

Title:

Control Method and Apparatus for Testing of Multiple

Processor Integrated Circuits and Other Digital Systems

Group:

To Be Assigned

Examiner:

To Be Assigned

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicants' attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying Form PTO-1449. A copy of each listed document is enclosed.

- 1. D. Jaskolski, "How to Design an IDE for Debugging Multi-processor DSP Systems," DSP Engineering, pp. 1-17, June 2000.
- 2. Institute of Electrical and Electronics Engineers (IEEE) Standard 1149.1, "IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE, New York, NY, October 1993.
- 3. Institute of Electrical and Electronics Engineers (IEEE) Standard 1149.1b, "Supplement to IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE, New York, NY, March 1995.

It is believed that there is no fee due in conjunction with the filing of this Supplemental Information Disclosure Statement. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit Lucent Technologies Deposit Account No. 12-2325 as required to correct the error.

The filing of this Supplemental Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability, or as a representation that no other material information exists.

Respectfully submitted,

Joseph B. Ryan

Reg. No. 37,922

Attorney for Applicant(s)

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Date: July 24, 2000 Ryan & Mason, L.L.P. 90 Forest Avenue

(516) 759-7517

Locust Valley, New York 11560